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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,881	09/23/2003	Robin E. Gorrell	58053US005	3599
32692	7590	02/11/2008		
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EXAMINER				
CHU, CHRIS C				
ART UNIT		PAPER NUMBER		
2815				
NOTIFICATION DATE		DELIVERY MODE		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

LegalUSDocketing@mmm.com

LegalDocketing@mmm.com

Office Action Summary

Application No.

10/668,881

Applicant(s)

GORRELL ET AL.

Examiner

CHRIS C. CHU

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 October 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 - 8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 - 8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SF/ICE)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(c), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(c) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 31, 2007 has been entered. An action on the RCE follows.

Response to Amendment

2. Applicant's amendment filed on October 31, 2007 has been received and entered in the case.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gregor et al. (U. S. Pat. No. 5,354,955) in view of Ma (U. S. Pat. No. 6,448,639).

Regarding claim 1, Gregor et al. discloses in e.g., Fig. 1 a laminated flip-chip interconnect package (the package in Fig. 1) comprising

- a substrate (12; column 3, line 7) having a chip attach surface (the top surface of the substrate 12 where the chip 14 is attached) and an opposing board attach surface (the bottom surface of the substrate 12) that define contact pads (the pads under the solder ball 20 and pads on the top surface of the substrate 12) for attachment to corresponding pads on the chip (14; column 3, line 8) and board (10; column 3, line 5),
- wherein the board attach surface (at the bottom surface of the substrate 12) comprises
 - o a pattern of contact pads (the pads under the solder ball 20) opposite and “adjacent” a chip attach location (the area on the substrate 12 where the chip 14 is attached) on the chip attach surface except at least one unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) of the board attach surface (see e.g., Fig. 1),
 - o said unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) being “adjacent” to a corner of chip attach location (see e.g., Fig. 1), and
- said board attach surface (the surface that has the elements 120) comprising a dielectric material (the lowermost dielectric layer in the element 12). As shown in e.g., Fig. 1 of Gregor et al., the unpatterned solid plane area (at the solid and non-pad

areas on the back surface of the element 12 which are directly opposite areas of the element 25) has at least the size of a region.

Gregor et al. doesn't explicitly state that the unpatterned solid plane area extends a distance equal to at least two contact pad rows beyond the corner of the chip attach location for a distance equal to at least two contact pad rows and extends under the corner of the chip attach location for a distance equal to one contact pad row. Ma teaches in e.g., Fig. 1 and Fig. 2 an unpatterned solid plane area (the area that does not have elements 110; see e.g., Fig. 2) extending a distance equal to at least two contact pad rows (110; column 1, lines 32 and 33) beyond the corner of a chip attach location (101; column 1, line 18 and see e.g., Fig. 2) for a distance equal to at least two contact pad rows (see e.g., Fig. 2) and extending under the corner of the chip attach location (101) for a distance equal to one contact pad row (see e.g., Fig. 1). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the diameter of the unpatterned solid plane area of Ma to form the specific diameter of the unpatterned solid plane area of Gregor et al. as taught by Ma to reduce the thermal stresses on the solder joints created by the CTE mismatch between the substrate and the chip (column 1, lines 55 – 58).

Regarding claim 4, Gregor et al. discloses in e.g., Fig. 1 a laminated flip-chip interconnect package (the package in Fig. 1) comprising

- a substrate (12) having a chip attach surface (the top surface of the substrate 12 where the chip 14 is attached) and an opposing board attach surface (the bottom surface of the substrate 12) that defines a pattern of contact pads (the pads between the solder

ball 20 and the substrate 12) for attachment to corresponding pads on the chip (14) and board (10),

- wherein the board attach surface (at the bottom surface of the substrate 12) comprises
 - o at least one unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25),
 - o said unpatterned area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) being opposite a chip attach surface region adjacent at least one corner of a chip attach location (see e.g., Fig. 1), and
- said board attach surface comprising a metal (At the year 1994, all wirings or circuits or pads materials includes metal materials, i.e., copper or aluminum, etc. Thus, Gregor et al. meets this limitation.). As shown in e.g., Fig. 1 of Gregor et al., the unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) has at least the size of a region.

Gregor et al. doesn't explicitly state that the unpatterned solid plane area extends a distance equal to at least two contact pad rows beyond the corner of the chip attach location for a distance equal to at least two contact pad rows and extends under the corner of the chip attach location for a distance equal to one contact pad row. Ma teaches in e.g., Fig. 1 and Fig. 2 an unpatterned solid plane area (the area that does not have elements 110; see e.g., Fig. 2) extending a distance equal to at least two contact pad rows (110; column 1, lines 32 and 33) beyond the

corner of a chip attach location (101; column 1, line 18 and see e.g., Fig. 2) for a distance equal to at least two contact pad rows (see e.g., Fig. 2) and extending under the corner of the chip attach location (101) for a distance equal to one contact pad row (see e.g., Fig. 1). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the diameter of the unpatterned solid plane area of Ma to form the specific diameter of the unpatterned solid plane area of Gregor et al. as taught by Ma to reduce the thermal stresses on the solder joints created by the CTE mismatch between the substrate and the chip (column 1, lines 55 – 58).

5. Claims 2, 3 and 5 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gregor et al. and Ma as applied to claims 1 and 4 above, and further in view of Lau (U. S. Pat. No. 6,075,710).

Regarding claims 2, 3 and 5 – 7, while Gregor et al. and Ma disclose the use of the dielectric and metal materials on the board attach surface of the substrate, Gregor et al. and Ma do not disclose a solder mask on the dielectric material (claim 2) and metal (claim 6), the solder mask being a polyimide (claims 3 and 7) and the metal material being copper (claim 5). Lau teaches in e.g., Fig. 4A a solder mask (155 or 235; column 5, lines 65 – 67) on a dielectric material (the dielectric material in the bottom of the substrate; column 5, lines 19 and 20) and metal (Cu 130; column 5, lines 38 – 40) and the solder mask being a polyimide (column 7, line 39. Since the element 235 of Lau works as a mask layer for the solder pastes 245, the element 235 reads as a solder mask. Since the solder mask 235 is made by a polyimide material, Lau discloses a polyimide material for the solder mask). It would have been obvious to one of

ordinary skill in the art at the time when the invention was made to further apply the solder mask (e.g., polyimide) of Lau to cover the dielectric material and metal on the unpatterned solid plane area of Gregor et al. and Ma as taught by Lau to provide finer pitches between the external connections (column 6, lines 4 – 6).

Regarding claim 8, Gregor et al., as modified, discloses a solder mask (155 of Lau) having a plurality of openings (the openings for the pads 130 of Lau) defining ball grid array pads (see e.g., Fig. 3C).

Response to Arguments

6. Applicant's arguments with respect to claims 1 and 4 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRIS C. CHU whose telephone number is (571)272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Chris C. Chu
Primary Examiner
Art Unit 2815

/Chris C. Chu/
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Tuesday, January 29, 2008